tic including multiple independently planarized layers of dielectric material therein, said multiple independently planarized layers including a lower portion of a spin-on glass a middle portion of a dielectric material which is not spin-on glass, and an upper portion of spin-on glass;

a third patterned thin-film layer comprising substantially undoped polysilicon having a very high resistivity;

wherein said first patterned thin-film layer is configured to provide transistor gates, and said first and second thin-film layers are interconnected to provide an array of latches, and said third thin-film layer overlies said patterned interlevel dielectric and is interconnected through contact holes with said first and second layers to provide resistive loads for each said latch.

2. The integrated circuit of claim 1, wherein said first thin-film layer also comprises a silicide cladding.

3. The SRAM cell of claim 1, wherein said interlevel dielectric comprises two layers of spin-on glass.

4. The SRAM cell of claim 1, wherein said interlevel dielectric also comprises at least two dielectric layers which are not planarized.

5. The SRAM cell of claim 1, wherein said second interlevel dielectric comprises at least four layers.

6. The SRAM cell of claim 1, wherein said loads each have a resistance value of about 1TΩ.

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7. An integrated circuit SRAM cell, comprising:

first and second overlaid thin-film conductor layers, each comprising clad polysilicon; at least one of said conductor layers being capacitively coupled to substantially monolithic semiconductor material to define field-effect transistor channels therein;

a patterned interlevel dielectric overlying portions of said second thin-film layer, and including multiple independently planarized layers of dielectric material therein, said multiple independently planarized layers of dielectric material including at least three different layers of dielectric material, with at least two of said layers of dielectric material being independently planarized layers of pin-on glass;

a third patterned thin-film layer comprising substantially undoped polysilicon having a very high resistivity, and lying on a substantially planar top surface of said patterned interlevel dielectric;

wherein said first patterned thin-film layer is configured to provide transistor gates, and lust and second thin-film layers are interconnected to provide an array of latches, and said third thin-film layer overlies said patterned interlevel dielectric and is interconnected through con-

tact holes with said first and second layers to provide passive loads for respective ones of said latches.

8. The SRAM cell of claim 7, wherein said interlevel dielectric comprises two layers of spin-on glass.

9. The SRAM cell of claim 7, wherein said interlevel dielectric also comprises at least two dielectric layers which are not planarized.

10. The SRAM cell of claim 7, wherein said interlevel dielectric comprises at least four layers.

11. The SRAM cell of claim 7, wherein said loads each have a resistance value of about 1TΩ.

12. An integrated circuit SRAM cell, comprising:

at least one patterned thin-film conductor layer comprising polysilicon and being capacitively coupled to substantially monolithic semiconductor material to define field-effect transistor channels therein;

a patterned interlevel dielectric overlying said thin-film conductor layers, and including multiple independently planarized layers of dielectric material therein, said multiple independently planarized layers of dielectric material including at least three different layers of dielectric material, with at least two of said layers of dielectric material being independently planarized layers of spin-on glass;

an additional patterned thin-film layer comprising substantially intrinsic polysilicon, and lying on a substantially planar top surface of said patterned interlevel dielectric;

wherein said patterned thin-film conductor layer are interconnected to provide an array of latches, and said additional thin-film layer overlies said patterned interlevel dielectric and is interconnected through contact holes with said conductor layers to provide passive loads for respective ones of said latches.

13. The SRAM cell of claim 12, wherein said additional layer comprises SIPOS.

14. The SRAM cell of claim 12, wherein said additional layer comprises polysilicon doped with chlorine.

15. The SRAM cell of claim 12, wherein said interlevel dielectric comprises two layers of spin-on glass.

16. The SRAM cell of claim 12, wherein said interlevel dielectric also comprises at least two dielectric layers which are not planarized.

17. The SRAM cell of claim 12, wherein said interlevel dielectric comprises at least four layers.

18. The SRAM cell of claim 12, wherein said loads each have a resistance value of about 1TΩ.

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